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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,749	03/16/2004	Takashi Saiki	042193	1173
38834	7590	09/07/2005	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			HOANG, QUOC DINH	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

**Office Action Summary**

Application No.

10/800,749

Applicant(s)

SAIKI ET AL.

Examiner

Quoc D. Hoang

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 July 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
     Paper No(s)/Mail Date 3/16/04.
- 4) ☐ Interview Summary (PTO-413)  
     Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Election/Restrictions***

1. Applicant's election without traverse of Group I (claims 1-5) in the reply filed on 07/26/2005 is acknowledged.
2. This office action acknowledges receipt of the following items from the Applicant:
  - The Claims filed on 03/16/2004.
  - The Specification filed on 03/16/2004.
  - The Drawing filed on 03/16/2004.
  - The Abstract filed on 03/16/2004.
  - The Oath/declaration filed on 03/16/2004.

***Oath/Declaration***

3. The Oath/declaration filed on 03/16/2004 is acceptable.

***Priority***

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

5. The information disclosure statement (IDS) filed on 03/16/2004. The references cited on the PTOL 1449 Form have been considered.

***Specification***

6. The specification has been checked to the extent necessary to determine the present of all possible minor errors. However, Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Cheng et al (US Pub No. 2004/0266122, hereinafter "Cheng").

**Regarding claim 1**, Cheng teaches a semiconductor device comprising:

a gate 4 formed over a semiconductor region 1 while placing an insulating film 2 in between ([0020], Fig. 1 and Fig. 5);

a first impurity-diffused region 8 formed, as being aligned with said gate 4 in the surficial layer of said semiconductor region 1 ([0021], Fig. 1 and Fig. 5). *It is noted that the surficial layer is considered the silicon layer formed on the silicon-on-glass semiconductor region 1;*

a second impurity-diffused region 18 formed, as being distant from said gate 4 while placing a portion of a side of said first impurity-diffused region 8 in between ([0025], Fig. 3 and Fig. 5); and

a third impurity-diffused region 24 formed as being distant from said gate 4 while placing said portion of said side of said first impurity-diffused region 8 and a portion of a

side of said second impurity-diffused region 18 in between ([0029] and Fig. 5); wherein said second impurity-diffused region 18 is formed as containing a diffusion suppressive element ([0022] and [0025]). *It is noted that a dopant similar to the dopant (arsenic) employed to form the first impurity-diffused region 8 is considered the diffusion suppressive element.*

Cheng teaches the claimed invention except for “diffusion suppressive element for suppressing diffusion of an impurity contained in said third impurity-diffused region”. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to combine the second impurity-diffused region 18 containing a diffusion suppressive element (arsenic) teaching of Chang with “diffusion suppressive element for suppressing diffusion of an impurity contained in said third impurity-diffused region”, since it has been held that the recitation of a new intended use for an old product does not make a claim to that old product patentable, *In re Schreiber* 44 USPQ2d 1429 (Fed. Cir. 1997).

**Regarding claim 2,** Cheng teaches further comprising:

a first sidewall spacer 16 formed over both lateral faces of said gate 4 ([0025], Fig. 3 and Fig. 5); and

a second sidewall spacer 22 formed to cover said first sidewall spacer 16 over both lateral sides of said gate 4 ([0029] and Fig. 5); wherein said second impurity-diffused region 18 is formed as being aligned with said first sidewall spacer 16, and said third impurity-diffused region 24 is formed as being aligned with said second sidewall spacer 22 ([0021], [0030], and Fig. 5).

**Regarding claim 4**, Cheng teaches wherein the diffusion suppressive element is arsenic, where the impurity contained on the first and third impurity-diffused regions 8/18 is an n-type impurity ([0022], [0025], [0031], and Fig. 5). *It is noted that a dopant similar to the n-type dopant (arsenic) employed to form the first and third impurity-diffused region 8/18.*

**10.** Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al (US Pub No. 2004/0266122, hereinafter "Cheng") in view of Kim et al., (US Pat No. 6,275,906, hereinafter "Kim").

**Regarding claim 3**, Cheng teaches further comprising a fourth impurity-diffused region 6 formed, in the surficial layer of the semiconductor region 1, as being aligned with the gate 4 ([0021], Fig. 1 and Fig. 5), but does not clearly teach the fourth impurity-diffused region containing an impurity having a conductivity type opposite to that of impurities contained in said first and third impurity-diffused regions.

However, Kim teaches the fourth impurity-diffused region 26 containing an impurity having a conductivity type (p-type) opposite to that of impurities contained in said first impurity-diffused region (n-type) 22 and third impurity-diffused region (n-type) 28 (col. 3. lines 10-45 and Fig. 1). Since Cheng and Kim are all from the same field of endeavor, the purpose disclosed by Kim would have been recognized in the pertinent art of Cheng. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the fourth impurity-diffused region containing an impurity having a conductivity type opposite to that of impurities contained in said

first and third impurity-diffused regions in order to enclose the first impurity-diffused region and prevent the impurity from being inwardly extending beyond the first impurity-diffused region as taught by Kim, column 5, lines 1-18.

**11.** Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al (US Pub No. 2004/0266122, hereinafter "Cheng") in view of Hayashida et al., (US Pat No. 5,6903,029, hereinafter "Hayashida").

**Regarding claim 5**, Cheng teaches wherein the diffusion suppressive element is boron (p-type), where the impurity contained on the first and third impurity-diffused regions 8/18 is an p-type impurity, but does not clearly teach wherein the diffusion suppressive is at least any one element selected from germanium, nitrogen, fluorine, carbon and indium ([0022]).

However, Hayashida teaches an impurity to be implanted to form the high concentration region 9 is not limited to boron, but a different impurity having the same conductivity type (p-type) as that of boron, such as indium may also be used (col. 5, line 64 through col. 6, line 11 and Fig. 1). Since Cheng and Hayashida are all from the same field of endeavor, the purpose disclosed by Hayashida would have been recognized in the pertinent art of Cheng. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the indium as an p-type impurity instead of boron in order to easy to control the impurity concentration profile, since indium, in compared to boron, has a larger atomic weight, a smaller implantation range and a smaller diffusion coefficient as taught by Hayashida, column 6, lines 1-11.

***Conclusion***

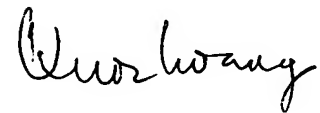
**12.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers of the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quoc Hoang

Patent examiner/AU 2818



08/21/2005